WHAT IS CLAIMED IS:

1. A semiconductor device having a multiple wiring layer structure, comprising:

a first conductive layer connected to a conductive member for external connection;

a second conductive layer disposed below said first conductive layer, the second conductive layer having a plurality of openings;

a third conductive layer disposed below said second conductive layer;

a first insulating interlayer disposed between said first conductive layer and said second conductive layer;

a first through hole provided in said first insulating interlayer;

a fourth conductive layer filling said first through hole;

a second insulating interlayer disposed between said second conductive layer and said third conductive layer;

a second through hole provided in said second insulating interlayer; and

a fifth conductive layer filling said second through hole.

2. The semiconductor device according to claim 1, wherein said first insulating interlayer and said second insulating interlayer are connected to each other through said openings of said second conductive layer, and a contiguous section of said first insulating interlayer with said second insulating interlayer is, thereby, formed between said first conductive layer and said third conductive layer.

3. The semiconductor device according to claim 1, wherein said second conductive layer has a planar network pattern.

4. The semiconductor device according to claim 1, wherein said third conductive layer is the lowest conductive layer formed on an insulating film covering a surface of a semiconductor substrate, and said third conductive layer is also provided with a plurality of openings.

5. The semiconductor device according to claim 4, wherein said third conductive layer has a planar network pattern.

6. The semiconductor device according to claim 1, wherein said conductive member for external connection is a bonding wire.

7. The semiconductor device according to claim 1, wherein said first conductive layer, said second conductive layer and said third conductive layer comprise aluminum as a major component, and said fourth conductive layer and said fifth conductive layer comprise tungsten as a major component.

8. The semiconductor device according to claim 1, wherein said semiconductor device further comprises an internal circuit, said internal circuit being formed by the multiple wiring layer structure, and said first conductive layer, said second conductive layer, said third conductive layer, said fourth conductive layer, said fifth conductive layer, said first insulating interlayer, said second insulating interlayer, said through holes, and said multiple wiring layer structure are formed by a collective production process.

9. The semiconductor device according to claim 1, wherein said semiconductor device further comprises a guard ring, said guard ring comprising:

a sixth conductive layer comprising the same material as said first conductive layer;

a seventh conductive layer comprising the same material as said second conductive layer;

an eighth conductive layer comprising the same material as said third conductive layer;

said first insulating interlayer and said second insulating interlayer;

a first groove provided on said first insulating interlayer;

a second groove provided on said second insulating interlayer;

a ninth conductive layer filling said first groove; and

a tenth conductive layer filling said second groove.

10. The semiconductor device according to claim 9, wherein said guard ring is formed around said multiple wiring layer structure.

11. The semiconductor device according to claim 9, wherein said guard ring is formed in a perimeter portion of the semiconductor device.

12. The semiconductor device according to claim 1, wherein the first and second through holes are axially aligned.

13. The semiconductor device according to claim 1, wherein the first and second through holes are axially offset.

14. The semiconductor device according to claim 1, wherein the fourth and fifth conductor layers do not overlap.

15. A method for making a semiconductor device having a multiple wiring layer structure connected to a conductive member for external connection, comprising:

(1) forming a first insulating interlayer on a first conductive layer;

(2) selectively forming through holes in said first insulating interlayer;

(3) embedding said first conductive material into said through holes;

(4) forming a second conductive layer on said first insulating interlayer so as to come into

contact with said first conductive material embedded into said through holes;

(5) forming a plurality of openings by patterning said second conductive layer;

(6) forming a second insulating interlayer on said second conductive layer having said plurality of openings;

(7) embedding second conductive material into through holes formed in said second insulating interlayer; and

(8) forming a third conductive layer on said second conductive layer so as to come in contact with said second conductive material embedded into said through holes.

16. The method for making a semiconductor device according to claim 15, further comprising:

depositing said first conductive material on said first insulating interlayer and in said through holes; and

etching said first conductive material.

17. The method for making a semiconductor device according to claim 15, further comprising:

depositing said second conductive material on said first insulating interlayer and in said through holes; and

etching said second conductive material.

18. The method for making a semiconductor device according to claim 15, wherein said plurality of openings of said second conductive layer forms a planar network pattern.

19. The method for making a semiconductor device according to claim 15, wherein a multiple wiring layer structure of an internal circuit of said semiconductor device is formed by steps (1) to (8).

20. The method for making a semiconductor device according to claim 15, wherein a guard ring is further formed by steps (1) to (8).

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